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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,496	11/09/2001	Fong Piau	FLEX1814	3412

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PENINSULA IP GROUP
2290 North First Street, Suite 101
San Jose, CA 95131

EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/053,496	PIAU ET AL.
	Examiner	Art Unit
	Midys Inoa	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 2003/0009607 A1) in view of Katayama et al. (US 2001/0007119 A1) and further in view of Chien et al. (US 2003/0033465 A1).

Regarding Claim 1, 9, and 17 Chen discloses a method of carrying out data transfers to and from a flash memory 202 performed by a flash controller 204 comprising the steps of:

Determining which interface specification is to be used to transfer data, address information, and control signals to and from a host device ("software method [or]... hardware method...", page 3, paragraph 0027);

Detecting a command sequence to be processed ("transferring code by two steps..." wherein the steps represent a command sequence, page 3, paragraph 0028);

Translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array (paragraph 0028); and

Executing the specified data transfer (paragraph 0027-0030).

In order for the system of Chen to complete a transfer operation, a sequence of commands must be processed and translated into a number of steps to follow for the execution of a transfer. Chen does not teach the flash memory having a number of flash memory arrays or partitioning the

arrays. Furthermore, Chen does not transfer to a memory array pair, but instead transfers to a RAM.

Katayama et al. discloses a file memory device comprising:

A flash memory device 5 containing a number of flash memory arrays (See Figure 3);

Detecting the presence and number of compact flash memory arrays wherein the detecting occurs when the system performs data distribution and it must determine into how many memory arrays to distribute the data (Abstract);

Initializing the controller, the plurality of flash memory arrays as well as other internal components ("activate communication unit... controller...", paragraphs 056 and 061); and

Partitioning each of the flash memory arrays wherein the memory arrays of Katayama are partitioned by being organized in a parallel arrangement of memory element groups. As it is visible from Figure 3, the flash memory 5 comprising of flash memory arrays could be external and removable, thus allowing the system to "insert and power" the flash memory when necessary. This is further supported by Katayama's system's need to activate the controller in order to access the flash memory 5 (paragraph 056). The data being transferred in Katayama is distributed through out the arrays through the use of a data distribution unit within the data control circuit. In the case where the flash memory were to be divided into only two memory arrays, the **data distribution unit would serve the purpose of transferring data to a memory array pair**. Such a scenario is explored in Figure 11 where the distribution of data for two memory groups (or memory arrays) is explored (Paragraph 101). The memory groups "a" and "b" are those memory arrays that make up the memory array pair. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the flash memory

partitioning and data transferring method of Katayama et al. with the system of Chen in order to give the system the added ability of interleaving data throughout the memory arrays, thus making the transfer of data faster. The combination of Chen and Katayama et al. does not disclose partitioning the flash memory arrays in accordance to the parameters of a configuration information table stored in a memory of the compact flash controller. Chien et al. discloses an IDE system in which an IDE controller 10 comprises a memory 10a and reads from its memory a **partition table ("configuration information table") and provides information from this table** to the ATA interface **in order to create virtual partitions in the disk drive device** 30 (Paragraphs 19 and 22). Chien discloses that the real disk drive device could be a flash memory storage device (Claim 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the partitioning table of Chien et al. with the combined system of Chen and Katayama et al. since it would allow for the flash memory system to work not only in memories that have been partitioned in hardware, but also in non partitioned memories which could later be partitioned virtually by the controller.

Regarding Claims 2-3, 10-11, and 18-19, Chen teaches a system in which there is a choice as to what interface to use for the movement of data. When the system is in a flash ROM programming mode, an IDE interface is used. When the system is dealing with task files, an ATA interface is in effect ("an ATA or IDE interface is selected", Page 2, paragraph 0019).

Regarding Claims 4,12 and 20, Chen teaches a system in which the host provides the flash controller with a write command (specified command sequence) which is interpreted by the controller (data transfer operative elements) and allows it to perform the necessary steps to write

data from the controller into the flash ROM, thus completing the data transfer operation (Page 3, paragraph 0030).

Regarding Claims 5, 13 and 21, Chen teaches a system in which the host provides the flash controller with a read command (specified command sequence) which is interpreted by the controller (data transfer operative elements) and allows it to perform the necessary steps to read data from the flash ROM and store it in a RAM that is accessible to the host, thus completing the data transfer operation (Page 3, paragraph 0031).

Regarding Claims 6, 14, and 22, Chen teaches a system in which a "LENGTH" register specifies the number of bytes that need to be transferred, thus allowing the flash controller to continue the transfer operation until the system receives or transfers the specified number of bytes. This is how the controller knows that the operation has been completed (Page 3, paragraph 003, lines 15-16 and paragraph 0031, lines 8-9).

Regarding Claims 7-8, 15-16, and 23-24, Chen's flash controller does not perform any write, read, or transfer operation until a command is received from the host. Therefore, essentially, the flash controller stops operation and waits for a request from the host before is resumes normal operation.

Response to Arguments

3. Applicant's arguments filed on June 24th, 2004 with respect to claims 1, 9 and 17 have been considered but are not persuasive.

Applicant argues that the Chen and Chien references are not valid prima facie references sicne they were published after the filing date of applicant's claimed invention. However, the references in question; with filing dates of June 10th, 1999 for Chen and August 8th, 2001 for

Chien; are valid references since they would be available for use under the rules of 102(e) and are therefore also valid references under 35 U.S.C 103(a).

In response to applicant's arguments against the Chien reference individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant argues that Chien et al. does not disclose "determining which interface specification is to be used for transferring data..." or "detecting memory arrays" or "partitioning memory arrays". The Examiner would like to point out that the teachings of Chien et al. are not being relied upon to teach the limitations argued by applicant, but instead Chien is being used to provide the teaching of a "configuration information table".

The teachings of "determining which interface specification is to be used for transferring data..." are being taught by Chen and the teachings of "detecting memory arrays" and "partitioning memory arrays" are being taught by Katayama et al.

In response to applicant's argument that there is no suggestion or teaching on how the ATA system adapter taught by Chien et al. would be connected with the apparatus of Katayama et al., the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that the examiner has combined an excessive number of references ("even the large number of references cited by the Examiner does not render applicant's method obvious..."), reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa

Midys Inoa
Examiner
Art Unit 2188

MI

Mano Padmanabhan

10/4/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER